UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/016,863	12/14/2001	Justus Kuhn	W&B-INF-908	5945

24131 7590 06/03/2004

LERNER AND GREENBERG, PA
P O BOX 2480
HOLLYWOOD, FL 33022-2480

EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/016,863	KUHN ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-11 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-10 is/are rejected.

7)☒ Claim(s) 11 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 December 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 5.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-11 are presented for examination.

Information Disclosure Statement

The information disclosure statement (IDS) submitted on December 14, 2001 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Drawings

The drawings were received on December 14, 2001. These drawings are acceptable.

Claim Objections

Allowable Subject Matter

Claim 11 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 102

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-10 are rejected under 35 U.S.C. 102(e) as being anticipated by Schmoelz U.S. Patent No. 6,752,403.

As per claims 1 and 8, Schmoelz teaches a system and method for calculating and analyzing redundancies for semiconductor memories, this includes providing a memory device with at least one memory chip. The memory chip has a redundancy calculation region. The memory chip is tested to determine failure addresses of failed components on each memory chip. The addresses of the failed components are input to the redundancy calculation region to compare the failure addresses to previous failure addresses stored in the redundancy calculation region to determine if new failures have been discovered. If a match exists between the previous failure addresses and the failure addresses, the failure addresses which match are terminated. Otherwise, the failure addresses are stored in the redundancy calculation region. By comparing addresses of new fails with those of previous fails, the present invention is capable of deciding on the type of fail (row or column) during testing. Consequently, very few events have to be stored and the log can be small (abstract, Figure 2, column 2 lines 12-50, column 4 lines 50-54).

As per claims 2, 3, and 9, Schmoelz teaches that each block, stores an xy address. Fail addresses x[ ] and y[ ] are input to the pipeline and wander down the stack trying to find a number of matches or trying to find the first unoccupied empty block. If an address match is found, the number of matches is incremented and the fail address is terminated. Otherwise the address passes to the next block and the process continues. An address match is determined if the stored address is the same address as the input address, or an address match is determined if the failed x (y) address describes a failed row (column) and the

address is stored in the memory describes a row (column), i.e., same row (column failure). (Figures 2 and 3, column 8 lines 1-13)

As per claims 4-6, Schmoelz teaches a minimum grain for redundancy calculation may include the following characteristics. In extremis, this could be a 1 cell by 1 block minimum grain. But, since redundancies usually come in larger widths (e.g. double wordlines (WL) and quadruple bitlines (BL) (for example, for 4 Mb segments, etc.), a fuse is preferably employed to fix several WLs, or several BLs. Consequently, it is preferable to immediately reduce the fail-information to grains of the same length and width as the redundancies (i.e. 2 cells.times.4 cells for example). A row is thereby defined equal in size to a row redundancy, and a column is defined equal in size to a column redundancy. Thus, a grain is an intersection of a row with a column. (FIGS. 5A and 5B show an example of a memory array with redundancies, to demonstrate grain size). An associative memory stores xy pairs plus flags, similar to accumulators. xy-pairs are addresses of failed minimum grains in the chip, block, segment, etc. Whenever an xy pair is presented to memory, i.e., a fail address is entered x[a], y[a], memory stores this address, if there is nonidentical xy-pair stored therein. Additionally, the number of x matches m[a] and the number of y matches n[a] is generated (this is the major difference from a normal associative memory) by inputting results from each comparator to decision logic. If the number of X-matches (m or m[ ]) is larger than M, the new element becomes a row entry , since there is insufficient column redundancies to fix the element anyway. The same holds for Y-matches (n or n[ ]). If there are more than N, the new element

becomes a column entry. After the completion of a test, superfluous single cell entries (covered by later row or column entries) have to be removed, and the residual events have to be efficiently assigned to the remaining redundant elements which are stored as M (redundancy rows remaining) and N (redundancy columns remaining). Comparators are employed to compare x y match counts (m[ ] and n[ ]) to M and N, respectively. (Column 5 lines 53-67, column 7 lines 9-30, Figures 1-3)

As per claim 7, Schmoelz teaches the device under test is in need of repair (must-repair) when the fail address has counted (N-1) x-matches or (M-1) y-matches. The number of these matches is counted in m[ ] and n[ ] which are transferred down the pipeline with the fail addresses. When the Nth (or Mth) match is detected (n=N or m=M), a column or row must be repaired. The current stored address where the M or N occurred is then converted to a column or row address where a repair is needed so that a redundancy may be employed for the repair. (Column 8 lines 14-22)

As per claim 10, Schmoelz teaches that the Add_Fail describes a pipelined fail_log. Each clock pulse equals one call of Add_Fail. If there is no fail event to be processed, Fail_Flag is FALSE, otherwise it is TRUE. (Column 13 lines 1-4 Figures 2 and 3)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
Art Unit 2133

Guy J. Lamarre
for

Albert DeCady
Primary Examiner